The new wording of exemption 14 is proposed as follows:

Lead in solders consisting of more than two elements for the connection between the pins and the package of microprocessors with a lead content of more than 80% and less than 85% by weight until 31 December 2010, and for the repair and reuse of products that were put on the market before 1 January 2011.

4.20.5 References

[1] Goodman et al. 2004, Technical adaptation under Directive 2002/95/EC (RoHS) – Investigation of exemptions, ERA 2004, document "era_technology_study_12_2004.pdf"

[2] Intel on ex. 14, Stakeholder document "Exemption-14_Intel_31_March_2008.pdf"

[3] AMD on ex. 14, Stakeholder document "Lead-free_Questions on Exemption 14_May21_2008_final.pdf"

[4] EICTA et al. on ex. 14, Stakeholder document "Exemption_14_EICTA_and-others_1_April_2008.pdf"

[5] Master et al., AMD, Stakeholder document "Effect of Pin Count on Device Defective Rate_May 21 08.pdf"

[6] Hewlett Packard; Stakeholder document "HP Letter to the Oeko Institut - Rev3.1.pdf"

[7] E-mails from Julian Lageard, Intel, received on 3 and on 10 October 2008 by Dr. Otmar Deubzer, Fraunhofer IZM

[8] EICTA stakeholder document "EICTA Position on Exemption 14 3rd Oct 2008.pdf"

[9] AMD stakeholder document "Letter to Dr Deubzer_IZM Oct 17 2008.pdf"

[10] EICTA stakeholder document "Letter to Dr Deubzer_IZM Oct 17 2008.pdf"

4.21 Exemption No. 15

"Lead in solders to complete a viable electrical connection between semiconductor die and carrier within integrated circuit Flip Chip packages"

This exemption was described and explained in details in the ERA report in 2004 [1].

4.21.1 Description of exemption

The exemption in its current wording allows the use of leaded solders for level 1 interconnects: the bumps and the solders used to attach the bumps to the chip carrier.

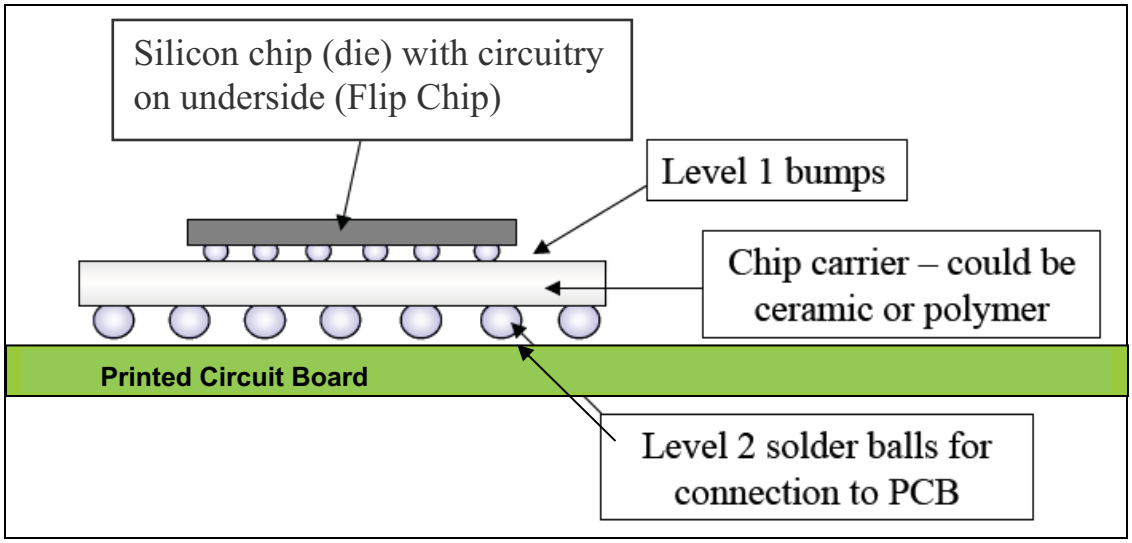


Figure 29 Flip chip package with ([1], modified)

The flip chip consists of the silicon chip, the underside circuitry and the bumps (balls on the underside). The bumps of the flip chip are connected to the contact areas of the chip carrier using a solder. Thus, a mechanical and electrical interconnect is formed between the flip chip and the chip carrier.

The flip chip and the chip carrier together form the flip chip package (FCP). These FCPs can be very complex, as the next figures show, with different die sizes and die thicknesses.

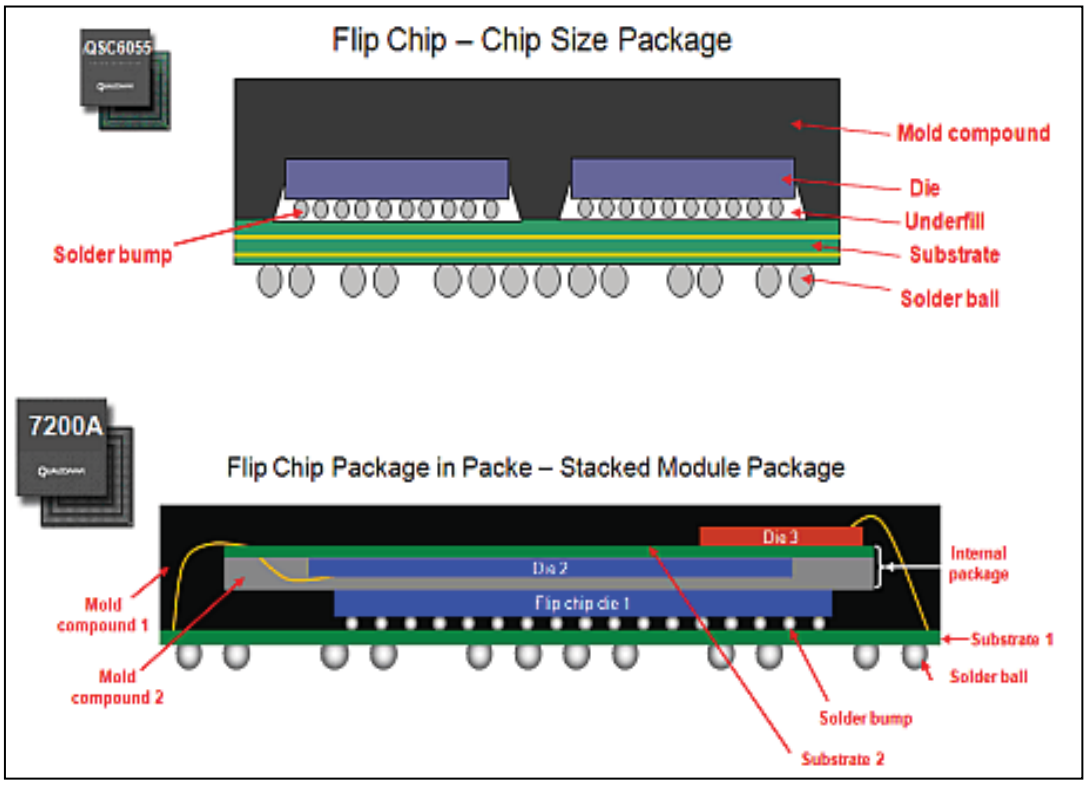


Figure 30 Schematic views of complex flip chip packages (small form factors, source: Qualcomm)

For the level 2 interconnects, lead-free solders can be used. For level 1 interconnects, different solders are applied [1]:

- High melting point solders with 85% and more of lead (e. g. 97%Pb3Sn, 90%Pb10%Sn)
- Lead-free solders, such as SnAg, Sn3.5%Ag0.7%Cu (SAC)
- gold, copper or gold tin
- eutectic solder (63%Sn37%Pb)

The solders used on level 1 in the flip chip connections must be [1]:

1. resistant to electromigration failure at the extremely high current densities required
2. able to create a solder hierarchy that allows staged assembly and rework of components in the manufacture process, and
3. have high ductility to reduce thermo-mechanical stress in under bump metallurgy (UBM) structures in particular in larger dies

Lead-free solders currently do not yet provide all these functionalities to a sufficient degree and hence are not appropriate to replace the leaded solders. Lead solders are in particular important for high reliability applications, large dies, and high performance applications with high current densities.

4.21.2 Justification by stakeholders

The stakeholders bring forward several arguments to justify the continuation of exemption 15. The arguments are summed up in the following sections.

Solder temperature hierarchy

Flip chip packages use high melting point solders with lead in order to achieve a solder hierarchy. They need a difference in the melting points of the solders applied on level 1 and level 2. Level 1 needs higher melting point solders in order to prevent the remelting of these solder joints during the soldering at level 2. The use of leaded solders with varying lead contents allows the adjustment of the melting points for the solders at level 1 depending on the requirements of the flip chip package or the production of the total device. [3]

Thermal mismatch

According to EICTA et al. [3], lead solders in the first level interconnects offer advantages that the current lead-free solders cannot provide. The core problem is the thermal mismatch between the die and the carrier due to the different coefficients of thermal expansion (TCE), and the resulting deformations as shown in the following figure.

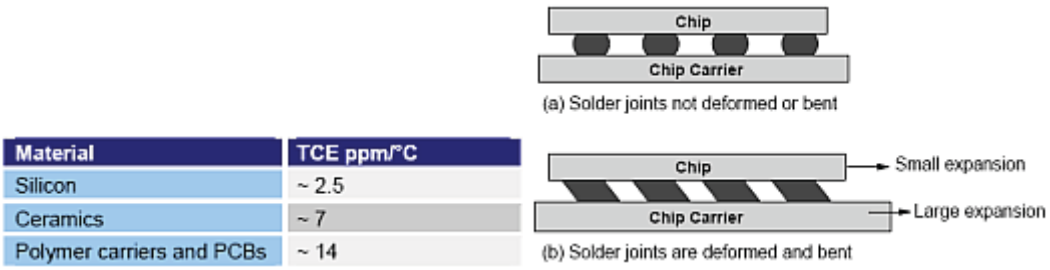


Figure 31 Coefficients of thermal expansion (TCE) and resulting deformation due to thermal mismatch [1]

The thermal mismatch problem increases with growing die diagonals. The differences in the thermal expansion coefficients become more effective in larger packages. The thermal stress increases with increasing distance of the bump to the centre of the die (distance to neutral point), and the most distant bumps thus contribute most to the mechanical stress on the die.

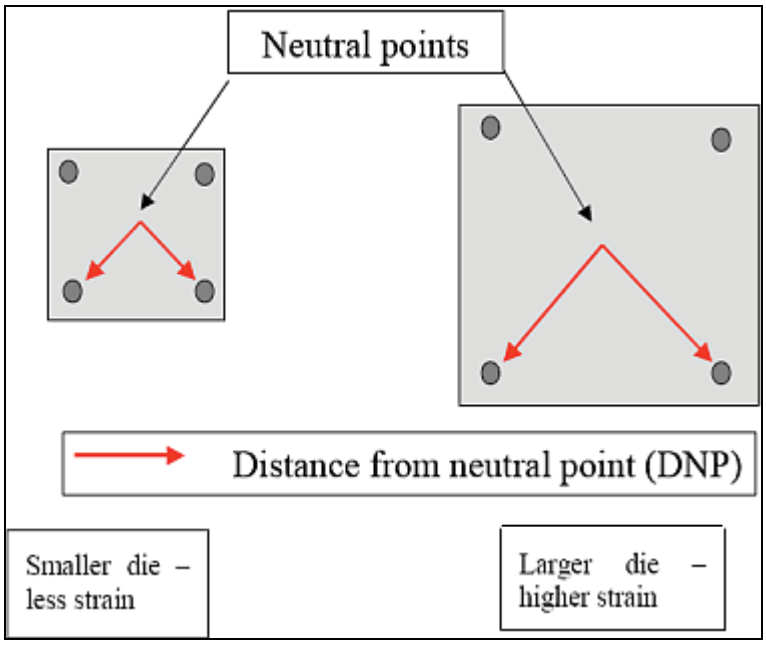


Figure 32 Increasing stress with increasing distance of the solder joint from the neutral point [4]

According to Xilinx [4] strain is imposed by several mechanisms including device fabrication. It is particularly severe however when the component's temperature changes as a result of differential thermal expansion. When temperature increases, the laminate expands more than the silicon and this applies a strain to the solder bump and to the materials to which these are attached. This strain can cause damage to:

- the dielectric material that is used as insulating layers on the silicon die surface, especially if low-k dielectric materials are used;
- the solder bonds to silicon die and to carrier circuit as a result of thermal fatigue;
- the silicon itself which may crack.

As the silicon die and carrier PCB are rigidly held by the solder bumps, the effect of differential thermal expansion is to apply an outward strain on the solder bump bonds. The applied force is partly relieved by distortion of the silicon and PCB which can "bow" outwards similarly to a "bimetallic strip" which bends when heated as a result of the different TCE values of the two metals. Therefore, as the expansion of the polymer laminate is constrained by the low TCE silicon, this results in warping of these two materials. Warping causes tension on joints which can cause cracking. Under-fill materials are injected between the die and carrier to reduce strain imposed on solder bumps by spreading out the forces induced by differential thermal expansion. [4]

Underfills are designed to put solder bumps into compressive strain which prevents fatigue failure but they also increase the overall stress to the package because they have larger TCE

values than the carrier material and this causes warping. The distortion from warping causes cracking and delamination of low k dielectrics and detrimentally affects the planarity of the level 2 solder balls. If the level 2 balls do not lie in a flat plane, some (usually those in the middle) will not make contact with the PCB causing open circuits. [4]

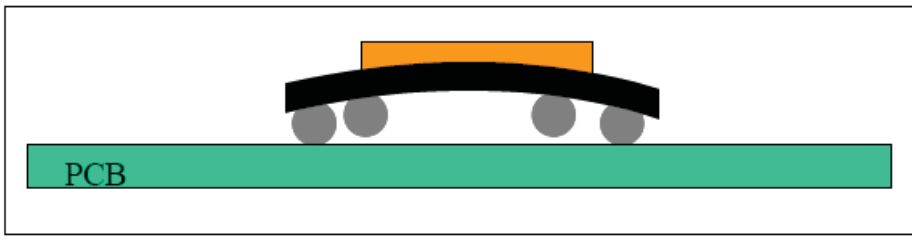


Figure 33 Warpage and effects on coplanarity of second level interconnects [4]

Research has shown that if the co-planarity of solder balls can be kept within 8 milli-inch (0.2 mm), good bonding to the printed wiring board is possible whereas worse co-planarity values indicate a high risk of open circuits. This value has been included in a standard published by JEDEC (Design Standard 95-1, section 14, June 2000). [4]

Lead-containing solders are ductile. Leaded solder joints absorb some of the tension between the silicon die and the ceramic or polymer carrier and hence protect the chip from fractures. Lead-free solders generally are stiffer and less ductile than lead-containing solders. The solder joint hence cannot compensate the thermo-mechanical stress. The tension from the thermal mismatch is directed into the chip, deforms the chip and can cause fractures. The thermal mismatch results in earlier failures of the lead-free flip chip package. In particular the low-k inner dielectrics in the die are prone to fractures, as they are brittle and are the weakest mechanical point in the die. [3]

Additionally, most lead-free solders have higher melting points. The elevated soldering temperatures require a strict control of the soldering profile, and even then it is not sure that the flip chip package will not be under residual stress after the soldering process: The materials expand to a different degree according to their thermal expansion coefficient, the solder melts and solidifies after the soldering process before all materials have returned into their normal expansion stage at room temperature. After the solidification of the solder joint, the materials (die, chip carrier) shrink, and the result is residual stress in the flip chip package after the soldering process. As lead-free solders solidify at higher temperatures, the die and the chip carrier are hotter at that time and hence change their thermal expansion more in returning to the original size compared to tin-lead solders. [3]

Electromigration

Most lead-free solders have a higher resistance than lead-containing solders. This may result in electromigration: material in the solder joint is dislocated from its original position due to the current passing through the solder joint. The result can be gaps and breaks in the solder joint, or voids, and in the end the failure of the solder joint. [3]

What is clear is that the electromigration effect increases with higher current densities. Smaller solder joints like the bumps in the flip chip in combination with the tendency towards higher performance devices exacerbate the electromigration problem for the flip chip packages. [1], [3]

Undercooling and reliability

Solidification of all tin (Sn) rich solder alloys, like the lead-free solders, requires the nucleation of Sn crystals from the melt. Sn crystals form in a low symmetry crystal structure with a very high activation barrier for nucleation. The further the melt temperature is lowered below the solidus temperature – the temperature at which the alloy is solid- the higher the thermodynamic driving force to overcome this activation barrier for the nucleation resulting in Sn grains in the solidified solder joint. [2]

Since homogenous nucleation in the melt is a stochastic process, it depends on the amount of Sn available. The probability of a nucleation event occurring therefore decreases with the volume of the melt. Thus, undercooling below the melting point is required for all Sn rich solder joints, but in small flip chip solder joints the level of undercooling required can be extreme. Undercooling as much as 60°C below the solidus temperature with tin-copper Pb-free alloys are documented. Problems with large undercooling of solder joints can occur when those joints arranged in large arrays as is the case for flip chip solder connections. The stochastic nature of significant undercooling to trigger Sn nucleation means that the solder joints in the array will be solidifying at widely varying times during the cool-down phase of the solder reflow operation. Packaging structures are not dimensionally stable during the temperature changes of reflow cool-down. Relative package distortions before final solidification of the array can create compromised solder joints at those few remaining solder joints that require the most extreme undercooling and are hence the very last to solidify. [2]

The undercooling effect and the resulting non-simultaneous solidification of solder joints hence is a problem increasing with the number of interconnects and with decreasing solder joint volumes in tin-rich solders, and is therefore a manufacturing-related reliability issue for flip chip packages. [2]

Impacts of SnAgCu microstructures on reliability and life time

After the soldering process, the “twinning” effect during cooling and solidification of high tin content solders, like most lead-free solders are, generates crystals in the solder joint with different steric orientation. The solidification and crystallization starts at a nucleation point and from there spreads into the solder joint. [3]

In flip chip bumps, the small volume makes it more probable that only one nucleation point exists. The result is that the solder joint is a single crystal. Crystals have a steric orientation, and the micromechanic properties in parts are dependent on the crystal orientation. This crystal orientation, however, may be different in each of the solder joints in a lead-free soldered flip chip. The result are bumps with more or less individual mechanical properties. Some of them, e. g., fail earlier than others under identical test conditions. The reliability and resulting life time of a lead-free soldered flip chip package hence are even more difficult or impossible to predict. The effect is in particular relevant for long life high reliability applications. [3]

Small solder volumes increase the “undercooling” effect during the soldering of lead-free solder joints, e. g. with tin-copper solders. Using silver containing lead-free alloys increases formation of large Ag_3Sn plates with complex effects on solder joint reliability. Such and other products of metallurgic reactions affect the mechanical properties of SAC solder joints as well as their reliability and life time. The formation of these products depends on the cooling rate after the soldering process, the solidification temperature, small deviations in the solder composition, annealing time and temperature, and the solder joint size. The complexity of the interference of all these factors result in solder joints whose properties cannot be fully predicted. Models to simulate the effects do not yet exist according to the stakeholders. Important material properties like the creep rate thus vary considerably between different solder joints. [3]

The SAC solder joint properties further on vary considerably and much more than SnPb joints during ageing and temperature cycling, and the effects are even stronger in small solder joints. The stakeholder say that in particular for high lead-free solder joints with their high tin contents, it is largely impossible yet to predict the reliability. [3]

The stakeholders conclude that the use of lead-free solders in flip chip bumps and solder joints thus is not yet possible in particular for high reliability applications.

Status and conditions for progress towards lead-free soldered flip chip packages

Table 10 gives an overview on the conversion towards lead-free level 1 interconnects.

Table 10 IBM Pb-free conversion roadmap estimate [source: IBM]

Pitch/Solder	Chip Size (mm)	Package	Current Density mA/khrs/°C	Node	Production
200µm Leaded	<21.5	Ceramic/NiP	250/100/100	65nm	2006
	<18.8	Organic/Eutectic	150/100/100	90nm	2007
150 Leaded	<14.7	Organic/Eutectic	100/100/100	65nm	2007
	<18.8	Organic/Eutectic	100/100/100	65nm	2008
200 Lead Free	<14.7	Organic/SAC	170/100/100	90nm	2006
	18.8	Organic/SAC	170/100/100	65nm	Tgt 2008
150 Lead Free	<14.7	Organic/SAC	170/100/100	45nm	2008
	<26	Organic/SAC	170/100/100	45nm	Tgt 2009
	<26	Organic/SAC	250/100/100	32nm	Tgt 2013
	<26	Ceramic/NiP	250/100/100	32nm	Tgt 2014

Note: this table has replaced the similar table from stakeholder document [3]. IBM had explained that the table in [3] is not correct and hence asked to replace it by the above version.
"Eutectic" indicates the use of SnPb37 solder containing 37% of lead per weight, "SAC" stands for lead-free tin-silver-copper solder.

The above roadmap, according to EICTA [3], is specific for IBM, but nevertheless representative of industry in general. The stakeholders abridge that the future "Pb-free Production" dates in the above table are estimates and targets. In many cases, invention is required for these dates to be achieved. Furthermore, these dates represent when Pb-free technology is estimated to be first commercially available. Additional transition time for qualification and implementation on specific products would be required.

The stakeholders [3] stated that the first small die organic packages were converted to lead-free solders in 2004, and the vast majority of components were released in preparation of the 1 July 2006 deadline in the RoHS Directive. In applications using small chips, it is advantageous to use organic chip carriers. All such packages have been converted to Pb-free solders, according to EICTA et al. [3]. On further inquiry into this statement, EICTA [6] confined it to refer to second level interconnects only. These solder joints, however, are not in the scope of this exemption and hence the above statement is obsolete.

The above table shows that smaller packages on organic carriers already use lead-free solders on first level are or will be converted to lead-free soldering in 2008 or 2009. Even several larger and more complex modules have been converted since then, but only around one year of experience is available, which according to [3] is short. Substitution of lead in the flip chip interconnect is currently underway for some other applications as well.

On the application side, previously promising alternatives have proven to be impractical in various high performance and / or high reliability applications. Some specific applications where lead solder is needed include those that require ceramic substrates and / or chips ≥ 14.7 mm on a side, ≥ 300 W, ≥ 100,000 POH (power-on hours), 100°C service temperature, and /or ≤ 65 nm pitch. [3]

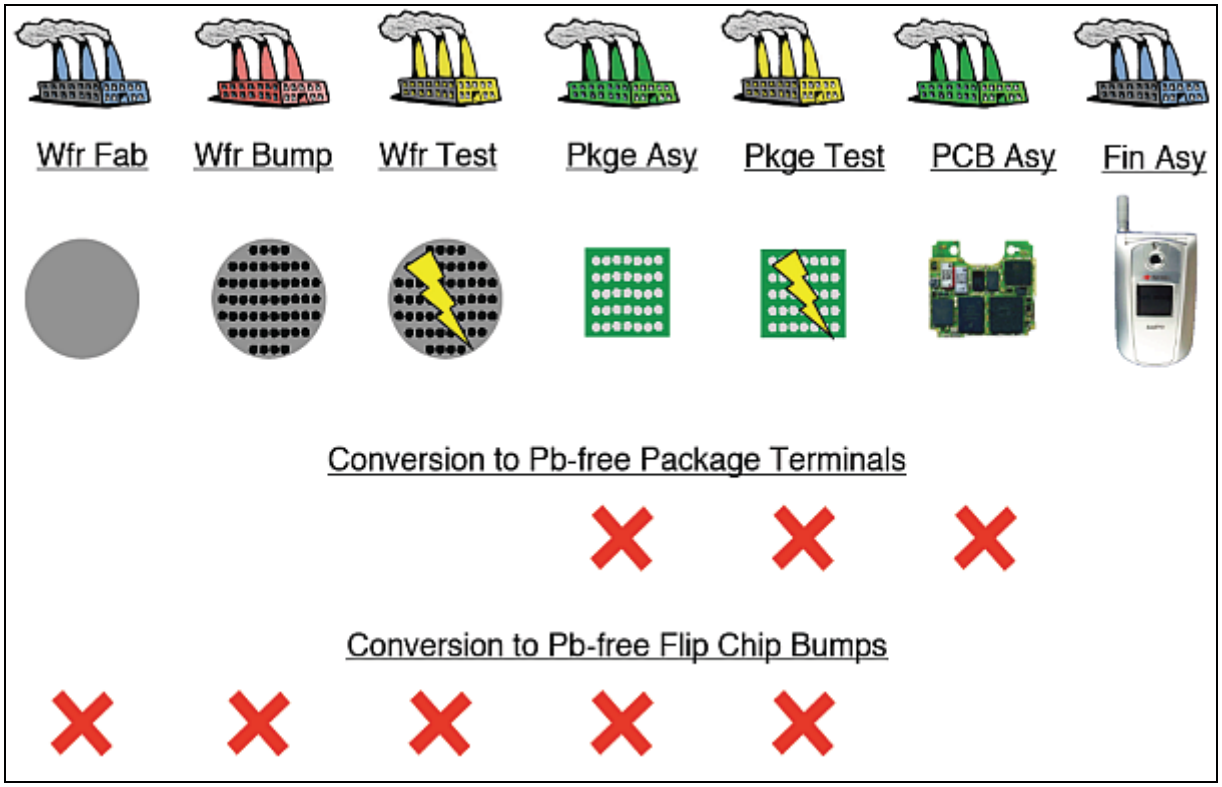
The stakeholders state that materials and design optimizations will be necessary which may require invention to overcome technical challenges such as electromigration, thermo-mechanical stress failure and to develop a solder melting temperature hierarchy. [3]

The stakeholder say that, as innovations are made in a particular application space (high reliability) or technology node (45 nm for example), they will be introduced to the market on an ongoing basis. These changes will preclude any back proliferation of these new lead-free flip chip technologies to older designs or technology nodes (65 nm, 90 nm etc). The stakeholders [3] state that some companies may be able to transition their products early (e. g. Xilinx [4]. Xilinx [4], a developer and manufacturer of reconfigurable chips known as field-programmable gate arrays (FPGAs), states that it will be possible by 2010 to produce flip chip devices with silicon die that are less than 17 mm along each side with lead-free solder bumps. For larger dies, this will not yet be possible by then.

According to EICTA [3], such individual company roadmaps do not represent the transition to Pb-free flip chip for the industry as a whole. They state that it is a complex technical issue, and because of the diversity of technologies and the time needed to validate reliability, it will take time for the entire industry to transition.

No single Pb-free bump solution is scalable across all flip chip technologies. There are many flip chip bump applications, including small thin packages and large high density packages. There are fine pitch and larger pitch bumps. Bumps are attached to many types of silicon die. Some products must survive routine high impact, while other products must survive constant minute vibrations. Flip chip package are used in high end servers, where they have to function reliably over long life of 10 years and more. They are also used in mobile phones, where they have to withstand shocks from dropping, vibrations and frequent temperature changes from switch on/off, but only over a short life time of a few years only. Each combination of density, package design, chip and substrate requires unique development as well as product and application specific qualification.

The shift from lead-containing towards FCPs using lead-free solders on the first level needs involvement and changes throughout the entire supply chain, as the figure below shows.



Note: Conversion ot Pb-free package terminals means the use of lead-free solders for second level interconnects; Pb-free flip chip bumps refer to the first level interconnects; Wfr: wafer; Asy: assembly

Figure 34 Involvement of the supply chain into conversion of FCPs to lead-free solders

The introduction of lead-free solders on the second level only needed the involvement of the supply chain starting with the package assembly, as the red crosses indicate in the above figure. Lead-free soldering on the first level is an interference requiring adaptations starting with the die up to the final assembly. Each wafer fab is working at specific technology nodes (45 nm, 60 nm, 90 nm, …) using specific production equipment and processing. Accommodating the various and partially conflicting requirements with lead-free solders in terms of thermo-mechanical stress, electromigration, manufacturability etc. needs new design rules in the wafer fab and in the following supply chain stages, the introduction of different dielectric materials, new material combinations on the die and carrier.

Additionally, each wafer fab has its own and very specific library of design rules and processing know how. This knowledge is competitive and will not be shared with others. As a consequence, each wafer fab requires an individual approach towards the conversion of lead-free soldering with the need of alignment with the other players in the supply chain. This is a further reason why it is not possible to draw a line where lead-free soldering is possible, and where it is not, besides the application aspects.

The stakeholders claim that for these reasons, the development of reliable lead-free FCPs for all the different applications takes time. Until the Pb-free flip chip process technology

matures and is proven reliable in all applications through product qualifications, RoHS exemption 15 will remain crucial for flip chip products, according to EICTA [5].

The stakeholders claim that for these reasons, the development of FCPs for all the different applications takes time.

Until the Pb-free flip chip process technology matures and is proven reliable in all applications through product qualifications, RoHS exemption 15 will remain crucial for flip chip products, according to EICTA [5].

Necessity of a transition period

Once lead-free alternative systems have been identified and are being brought to commercialization, EICTA et al. [3] suggest 24 to 60 months implementation time is necessary for qualification by the semiconductor manufacturer and by the system integrator for final product qualification.

According to EICTA et al. [3], the specific time required depends primarily on the level of reliability testing needed to confirm robustness for the target application. Factors affecting implementation time include:

(1) new equipment design, manufacture, delivery, installation and qualification times;

(2) raw material and fabricated component procurement lead times;

(3) process debug and implementation with proven quality control periods. There is not a fixed transition time for Pb-free implementation, according to EICTA et al. [3].

4.21.3 Critical review

Confinement of stakeholders' arguments

The stakeholders plausibly explain the constraints related to the use of lead-free solders for level 1 interconnects in flip chip packages. The use of lead-free solders imposes additional problems in manufacturing of flip chip packages (FCP) as well as in their application, as the stakeholders describe.

Not all the stakeholders' arguments, however, actually are valid. In FCPs using underfills, the solder hierarchy issue is less severe or not an issue in case the underfilling is done carefully. The underfill keeps the first level solders in place and shape if they remelt during the reflow process for the attachment of the FCP to the printed wiring board. The use of underfills is common in FCPs.

On further inquiry, the statement could not be confirmed that the higher resistance of lead-free solders should be the root cause for stronger electromigration in lead-free solders. Electromigration, according to IBM, is a phenomenon mainly related to the interfaces of the solder joints and the underbump metallization/finishes. The selection and combination of materials forming the interfaces is crucial, not the resistance of the solder joint, or at best

indirectly. Electromigration occurs with eutectic (SnPb37) solders as well, and it is not ultimately clear that lead-free solders perform worse in any case.

Restriction of exemption 15

Nevertheless, the stakeholders' arguments justifying exemption 15 make clear that the introduction of lead-free solders introduce new challenges difficult or currently even impossible to overcome. This applies to both the manufacturing as well as the application of lead-free FCPs. Lead-free FCPs cannot yet be manufactured neither for the whole of the FCP product range, nor for all applications where FCPs are integral and indispensable for the proper functioning and performance of state of the art products.

As lead-free FCPs nevertheless are available, the crucial question for this review process is whether and how far the use of lead on level 1 solder joints in flip chip packages can be limited to those applications where lead can not yet be substituted or eliminated.

EICTA [5] claims that the segmentation of FCPs or applications where lead-free solders can be used is not possible. The manufacturing and the use of lead-free soldered FCPs has to take into account many influencing and limiting aspects both on the manufacturing as well as on the application side, such as:

1. FCP-specifications
   a) Die size/edge length
   b) Die thickness
   c) Bump size
   d) Bump pitch
   e) Technology node
   f) Organic/ceramic carrier
   g) Dielectric material
   h) Materials, types and combinations of under bump metallization, finishes, solder
   i) With/without underfill
2. Application conditions
   a) Power/current density
   b) Hours on power
   c) Life time
   d) Reliability and operational requirements
   e) Application specific thermal and/or mechanical impacts

Nevertheless, Xilinx [4] claimed that by 2010 it should be possible to manufacture FCPs with less than 17 mm of die length with a reliability, which is lower than for the lead-containing FCPs, but sufficient. Xilinx was asked whether FCPs with less than 17 mm length dies could be excluded from exemption 15, and whether the die size actually would be a sufficient parameter to limit the exemption. No answer was received, and this stakeholder comment hence could not be taken into further account. Despite of this claim, Xilinx, however, supports the other stakeholders' arguments.

Based on the information submitted and confirmed by the stakeholders, a restriction of exemption 17 seems not to be possible in a way that would accommodate the technical situation as well as the need for a clear and manageable exemption wording. Opposing views of other stakeholders are not available.

Setting an expiry date

Simple and even more complex lead-free FCPs are available already, and their numbers will increase in the coming years. Art. 5 (1) (b) in this case requires the limitation of the exemption to those cases, where the use of lead in FCPs is technically impracticable. The stakeholders, however, explained that the restriction of exemption 15 to certain types and/or applications of FCPs is not possible due to the technical complexity.

To adapt exemption 15 to the technical and scientific progress, it is recommended to set an expiry date equivalently to other exemptions with a similar situation, like e. g. exemption 7b.

Time is required on one hand for the production start and qualification of the lead-free flip chip packages once the concept and design is available. The stakeholders [3] indicate a minimum of 24 months from this time on to prepare and start up full production and for a complete qualification along the whole supply chain into specific applications.
On the other hand, time is necessary to convert and further develop existing lead-containing FCPs into lead-free ones, or to develop completely new packages. Based on the information available, it is not yet clear when this can be achieved across the entire FCP product and application range. In any case, the time required for the qualification of these packages would add to the time when the lead-free FCP is available.

The reviewers hence recommend the expiry date 31 July 2014. According to the stakeholders, it is not yet be clear whether at this time in the future actually all FCPs will have been fully converted to lead-free solders. In this case, however, either the stakeholders can apply for the continuation of the exemption in its current wording, or the exemption can be adapted to the state of the art at that point in time. The situation might be different from now and allow such restrictions.

4.21.4 Recommendation

Based on the available information from stakeholders', and in the absence of opposing views, the overall situation justifies the continuation of the exemption in line with Art. 5 (1) (b).

Lead-free flip chip packages are on the market. Art. 5 (1) (b) in this case requires the limitation of the exemption to those cases, where the use of lead in FCPs is technically impracticable. The technical complexity, according to the stakeholders, makes it impossible to restrict the exemption.

Instead of restricting the exemption, the consultants therefore recommend the expiry of the exemption on 31 July 2014. Additionally, the new exemption wording should allow repair and reuse of equipment put on the market before the expiry of the exemption.

The new wording is proposed as follows:

Lead in solders to complete a viable electrical connection between semiconductor die and carrier within integrated circuit flip chip packages until 31 July2014, and for the repair, or to the reuse, of electrical and electronic equipment put on the market before 1 August 2014.

4.21.5 References

[1] Paul Goodman et al., Technical adaptation under Directive 2002/95/EC (RoHS) – Investigation of exemptions; final report Dec. 2004;
Document "ERA Report 2004-0603.pdf"

[2] EICTA stakeholder document "EICTA Position on RoHS Exemption 15 8th August 2008.pdf"

[3] EICTA et al. on ex. 15; Stakeholder consultation document "Exemption_15_EICTA_and-others_1_April_2008.pdf"

[4] Xilinx stakeholder consultation document "Exemption15-Xilinx_Report_13_March_2008.pdf"

[5] EICTA stakeholder document "EICTA Position on Exemption 15 14th Oct 2008.pdf"

[6] Stakeholder document "RoHS v3.pdf", submitted by AMD, Freescale, IBM, Intel, Qualcomm and Texas Instruments