European Automobile Manufacturers Association (ACEA) · CLEPA European Association of Automotive Suppliers · JAMA Japan Automobile Manufacturers Association, Inc. · kama

9th Adaptation to scientific and technical progress of Exemptions 8(e), 8(f)(b), 8(g), 8(j) and 14 of Annex II to Directive 2000/53/EC (ELV), Stakeholder Consultation Questionnaire

Application for a continuation of Annex II ELV directive Exemption No. 8(g)
"Lead in solders to complete a viable electrical connection between semiconductor die and carrier within integrated circuit flip chip packages"

With this application the automotive industry, represented by their associations ACEA, CLEPA, JAMA, KAMA, et al. asks to extend above mentioned exemption with commitment to further develop Lead-free alternatives and for a further revision in 2024.

In this section we take reference to the questionnaire[i] from OEKO Institute published on May 29th 2018.

Abbreviations and Definitions

ELV Directive	Directive 2000/53/EC
FCP	flip chip package

Questions (Answers in blue color)

1. Please explain whether the use of lead in the application addressed under Exemption 8(g) of the ELV Directive is still unavoidable so that Art. 4(2)(b)(ii) of the ELV Directive would justify the continuation of the exemption. Please be specific with your answer, for example clarify, if applicable, what types of vehicles your answer refers to, i.e., conventional vehicles and various types of hybrid and electric vehicles, and which functionalities and applications the exemption still needs to cover.

   <Answer 1>
   Lead use, such as in a semiconductor device with high Lead bumps, are less rigid and can absorb a part of the stress induced during package assembly and during the board mounting process. Pb-free solutions are not able to meet these capabilities to date and fail standard qualification requirements. For vehicles, there are additional long-term reliability requirements under the harsh environmental conditions according to automotive specifications (e.g.AEC-Q100²) that need to be assessed and qualified according to automotive specifications. Further examples and details can be seen in response to Question #3.

The continuation of this exemption is required for all automotive models being designed, produced and currently on the market. Examples of applications used in vehicles are listed but not limited to the below:

- Electronic stability control systems
- Advanced emergency braking systems
- Distance control
- Lane departure warning systems
- Frontal projection systems
- Pedestrian protection
- Tire pressure monitoring systems to reduce rolling resistance and noise emissions
- Hydrogen and hybrid cars
- Car radio
- Vision systems
- Car-infotainment
- Traffic sign recognition
- Navigation
- Telematics
- Head-up displays

2. Can the wording of exemption 8(g) be aligned with the wording proposed for the equivalent exemption 15 of RoHS-Annex III (see specification above under ‘Background’)?

<Answer 2>
The current wording of the ELV 8(g) is exemption is:

Lead in solders to complete a viable electrical connection between semiconductor die and carrier within integrated circuit flip chip packages.

The exemption shall be reviewed in 2019.

The review of this exemption by the Commission within the RoHS review process likely did not provide every use case requiring the continuation of Lead use in flip chip applications that were requested by the exemption extension technical team. This is a concern of the ELV 8(g) Pilot team that all use cases must be listed in the future.

ELV is not directly comparable to RoHS due to different product scope, covered applications and product use profiles. We therefore ask to keep current ELV annex II wording as cited above, as this covers following essentially required characteristics, at least:

- Greater Than or Equal to 90nm semiconductor technology node
- Die size greater than or equal to 300mm^2 in any semiconductor technology / node (including stacked die)

- Stacked Die Packages using interposers greater than or equal to 300mm^2
- High current products (Rated at greater than or equal to 3amps) that use smaller package designs (With die sizes less than 300mm2) incorporating the flip chip on leadframe (FCOL) interconnect.

3. Please explain the efforts your organisation has undertaken to find and implement the use of lead-free alternatives for automotive uses. Please refer to alternatives, which at least reduce the amount of lead applied or eliminate its necessity altogether.

<Answer 3>

There is no direct Pb-free solution available for legacy packages requiring exemption 8(g) for most companies. The Lead (Pb) used in these packages resolved failures such as delamination, die crack and bump cracking being seen by any other solution when designed 10 or more years ago.

Pb-free efforts were focused on package redesigns that have increased the overall component's diameter, thickness and/or ultimately mass compared to the previous Pb containing packages. Since the newer package solutions cannot maintain the form, fit and function of the legacy package technology, they are not drop in replacements.

To achieve the basic 15-year service life of products in vehicles (post end of life for the vehicle's production), they must maintain Form, Fit and Function. Minor changes affecting these parameters cannot be ones that:

- Modify the devices height, width or length.
- Change how the connections from the device to the printed circuit board fit together.
- Significant material changes that can affect the functionality of the device in its current package design. Going from Lead to a non-Lead solution is a major material change.

If these devices were to be continually migrated to the latest IC fabrication process, the cost of designing new ICs and qualifying them in the systems would be prohibitive for many products.

The industry has demonstrated a strong commitment to developing new Lead-free flip chip devices as new technologies became available. Where it has not been feasible to move old designs into new IC technologies, the remaining devices present minimal risk to the environment. The remaining devices manufactured in leaded flip chip attach are expected to decline steadily over the next 5 years as those products are replaced with newer technology.

For the reasons outlined, the industry feels that an extension of at least 5 years is required for this exemption using the current wording. While the current form of the exemption is felt to be sufficient, the industry is willing to narrow the scope of the current exemption based to die size greater than 300 square millimeters or integrated circuit technologies greater than 90nm, and high current flip chip on leadframe (FCOL). Since many FCP products are used in high reliability applications, even if the exemption is

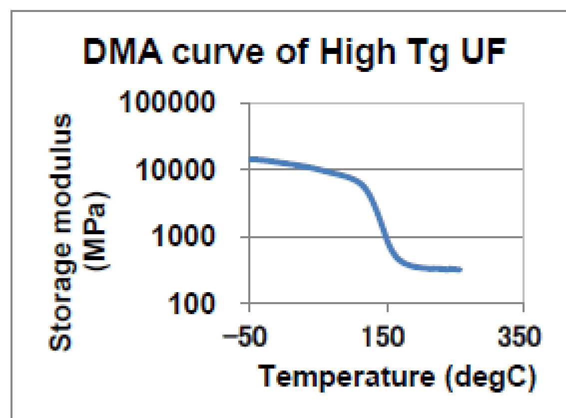
limited to large die size and older technologies, those FCP small die in new technology applications no longer under the exemption would need at least 36 months for customer qualification and supply chain transition. To eliminate this exemption for all devices prematurely would have significant socioeconomic risks associated with early retirement of critical technologies, placing EU countries at a competitive disadvantage.

The use of Lead-free solder bumps in flip chip interconnects continues to be a challenge. Reliability concerns are well documented with the use of Lead-free solders because they are less ductile than Lead solders. This causes the Lead-free solders to crack under stress and increases the likelihood for failures during the product life cycle. Preventing Lead-free solder cracks requires additional engineering to improve the thermal and mechanical fatigue life of the solder joints. The primary solution is a load-transfer from the solder to an underfill encapsulant. The residual stress from the underfill can cause other material failures which most commonly include dielectric crack, delamination or die crack. Each component must be redesigned and tested several times to obtain the correct formulation needed to protect each layer and the solder joints.

We recognize there are industry solutions available to prevent these failures for die sizes <300mm^{2}. However, solutions for large die sizes (>300mm^{2}) are not available due to the increased internal stresses that require more precise engineering to prevent the same failures from occurring. When using Lead-free solder with large die, we have experienced similar failures as previously mentioned, but we have also experienced less common failures as discussed below.

Large die with Lead-free bumps requires a high glass transition temperature (Tg>120°C) underfill (UF) to prevent solder bumps from cracking during stress tests. Figure 1 shows a typical high Tg UF with a large modulus (>10 GPa) at low temperature (<0°C). The DMA stress-strain curve shows that the storage modulus increases as the temperature decrease. The high Tg UF becomes very rigid at lower temperatures and the loss of flexibility places strain on the substrate solder mask.

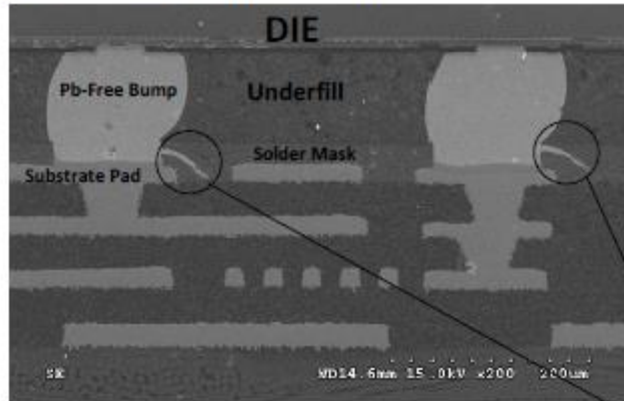
Figure 1



The solder mask layer is an organic polymer used for its insulating properties to prevent solder migration. The solder mask ensures a proper connection is made between the solder bump and substrate pad.

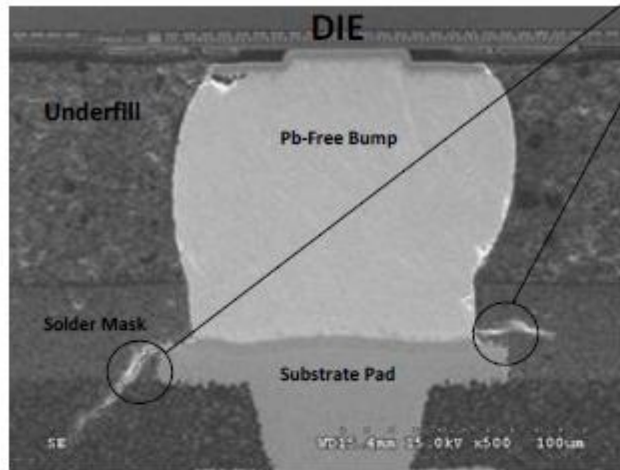
Figure 2 and Figure 3[ii] show that during reliability temperature cycling from -40°C to -50°C for large die the solder mask will crack due to the high stress imposed by the high Tg UF.

Figure 2: GPU (Sn/Ag bumps) ~350 mm²



Solder Mask Crack and Solder Extrusion

Figure 3: GPU (Sn/Ag bumps) ~500 mm²



The crack allows for solder to extrude through the solder mask. The solder extrusion significantly decreases the package reliability due to open-short failures.

The failures shown above demonstrate that the additional strain from large die increased the failure rate for the solder mask. Ultimately, this adds another variable to the equation in developing a solution to use Lead-free solder or any substitute interconnection technology for large die. Our research and development is still ongoing and more time is needed to find a long-term reliable Lead-free solution.

Challenges Associated with Large Stacked Die Flip Chip Package Assembly:

Figure 4 shows the schematic side view of a stacked silicon flip chip package. In this package, four active silicon die are connected to each other through a passive interposer with through silicon via (TSV) using micro-bumps. In this type of package, any number of active die can be assembled on the interposer and can then be connected to an organic package with C4 bumps. A capillary underfill is used to fill the gap between the micro-bumps and interposer, which helps in reducing the stress in micro-bumps. C4 bumps are created on the interposer backside, which are connected to a package substrate as shown in Figure 4. A second layer of C4 bump capillary underfill is used to fill the gap between the interposer, C4 bumps and the organic package.

Figure: 4 Schematic Side View of Stacked Die Package or Stacked Silicon Interconnect Package without Lid

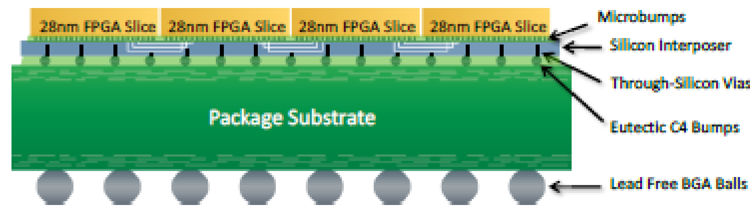
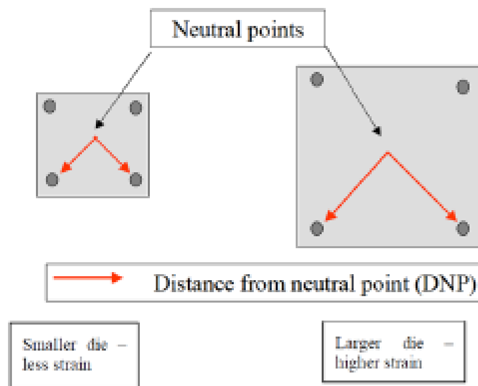


Figure 5: Dependence of Die Size on Level of Strain (Shown by Arrows) On Corner Bumps



Size of strain on bumps is dependent on the die size and the laminate material. Most laminates have similar thermal coefficient of expansion (TCE) which is ~15ppm/°C whereas silicon has TCE of ~2,5ppm/°C. The size of the strain on bumps located at opposite corners is proportional to die size. This is referred to as the distance from the neutral point (DNP), where there is no stress at the centre of the die.

Strain is imposed by several mechanisms including device fabrication. It is particularly severe however when the component's temperature changes as a result of differential thermal expansion.

When temperature increases, the laminate expands more than the silicon and this applies a strain to the solder bump and to the materials to which these are attached.

This strain can cause damage to:

- The dielectric material that is used as insulating layers on the silicon die surface, especially if low-k dielectric materials are used.
- To the solder bonds to silicon die and to carrier circuit as a result of thermal fatigue.
- To the silicon itself which may crack.

As the silicon die and carrier PCB are rigidly held by the solder bumps, the effect of differential thermal expansion is to apply an outward strain on the solder bump bonds as shown by the arrows in Figure 5. The applied force is partly relieved by distortion of the silicon and package, which can “bow” outwards similarly to a “bimetallic strip” that bends when heated as a result of the different TCE values of the two metals. Therefore, as the expansion of the polymer laminate is constrained by the low TCE silicon this results in warping of these two materials. Warping causes tension on joints which can cause cracking. Underfill materials are injected between the die and carrier package to reduce strain imposed on solder bumps by spreading out the forces induced by differential thermal expansion. Underfills are designed to put solder bumps into compressive strain which prevents fatigue failure, but they also increase the overall stress to the package because they have larger TCE values than the carrier material and this causes warping.

Eutectic Tin/Lead is a soft ductile alloy that forms strong bonds. High ductility is important as the solder deforms when a strain is imposed as a result of temperature due to the differential thermal expansion of silicon and carrier. Deformation of the eutectic Tin/Lead solder bumps when strain is imposed reduces the maximum level of strain on the solder joint and to the dielectric layers that form the circuitry on the silicon die. Calculations show that the maximum strain on joints imposed during thermal cycles when Tin/Lead solder is used is far lower than when the harder Lead-free solders are used.

Lead-free solders usually require underfills with higher Tg and higher modulus than eutectic solder. The main side effect of the higher Tg and modulus is that it imparts higher stress in the package and which results in higher overall package warpage. The room temperature co-planarity of a Lead-free stacked die package is almost two times higher than that of stacked die package with eutectic C4 bumps.

The distortion from warping causes cracking and delamination of low k dielectrics and detrimentally affects the planarity of the level 2 solder balls. If the level 2 balls do not lie in a flat plane, some (usually those in the middle) will not make contact with the PCB causing open circuits. The coplanarity of the Lead-free stacked die package is significantly higher than 8 mils. Research has shown that if the co-planarity of solder balls can be kept within 8 mil (0.2 mm) good bonding to the PCB is possible whereas worse co-planarity values indicate a high risk of open circuits. This value has been included in a standard published by JEDEC (Design Standard 95-1).[iii]

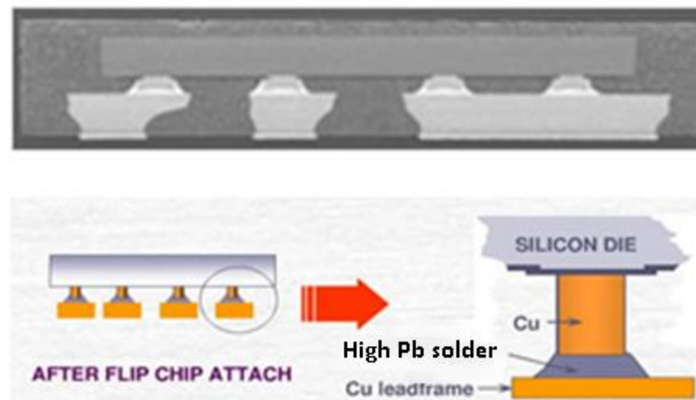
Challenges associated with Flip Chip on leadframe (FCOL)

Currently it is not possible to retrofit older Lead solder based FCOL parts into Lead-free solders. A brittle solder joint may drive 2 fail modes:

1. Strain transferred to the die may create cracked dielectric and metal lines
2. Solder joint is less robust and may crack, causing an electric open

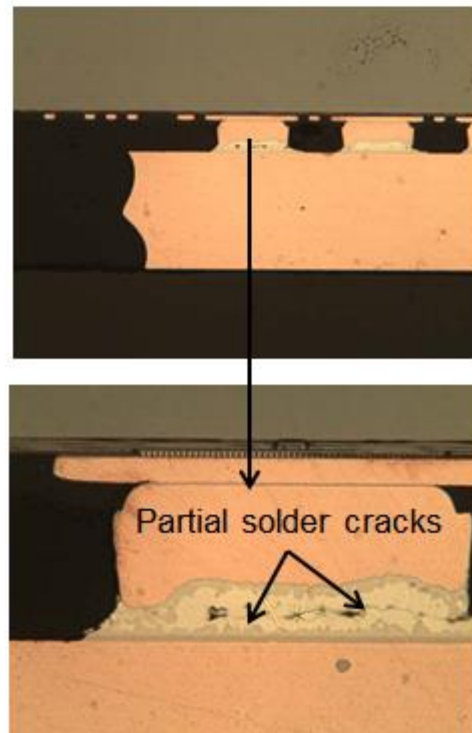
Failure rates have exceeded 20%. If pillar sizes are reduced to alleviate this stress, high current pillars will no longer meet electromigration limits.

Figure 6: FCOL package example



Going Lead-free, the solder joint becomes more brittle and requires a different set of design rules. The design rule changes would create a major change in package and die layout to convert from high-Lead to Lead-free. These types of major changes are not allowed for existing automotive products with expected long-term life requirements.

Figure 7: Solder crack failure of Pb-free solution under review



Flip Chip:
Alternatives are readily available for new silicon wafer fabrication technologies and small die sizes. These alternatives typically use Cu studs on the die and SnAg or SAC solder on the substrate. The Cu, SnAg and SAC are more rigid than the Pb flip chip solder, introducing more stress on the products. For older technologies, large die sizes, and large interposers for flip chip stacked die this additional stress ultimately results in an unacceptably high product failure rate.

Overmolded Flip Chip:
Lower temperature melting solder minimizes internal package stresses that prevent package failures such as package material interface delamination, i.e., the glue under the chip delaminates from the package substrate. Due to its high reliability characteristics, especially in mission critical applications, this solution must remain unchanged during the life of customer's product line. No new product designs will use the overmolded product solution.

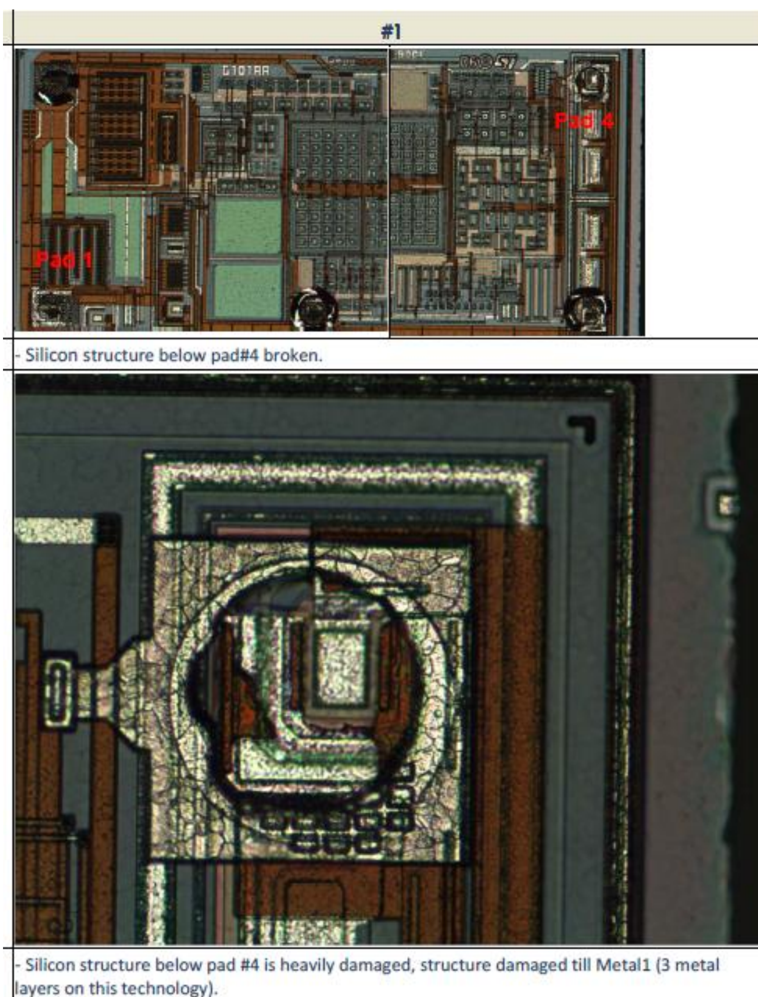
Flip Chip on leadframe:

The industry is working on Lead-free solutions, but none have been able to pass the same form / fit / function requirements met by the current Pb flip chip solution. Package is assembled on a Pb-free profile and the Pb internal solder joint using a 60% Pb solution does not melt during the secondary 260°C assembly process. By using the Pb internal solder joint, fatigue resistance to thermal cycling is much greater and resists cracking where Pb-free solutions currently fail.

Examples of recent research failure mechanism:

Recent research in automotive supply chain using a SnAg Sn= 96.5 % Ag = 3.5% Pb-free solution failed its basic qualification requirement for the maximum failure rate < 95 ppm (0.095%). The Lead-free bumped products experienced damaged silicon structure beneath the bump pads. Structural analysis concluded the damage was due to the mechanical stress applied on external leads when mounting the components on the boards. Current high Lead bumps are less rigid and can absorb a part of the stress induced during the package assembly process when the die is soldered on the leadframe and during the end customer's board mounting manufacturing process.

Figure 8: Failure Analysis of Silicon Damage – Pad # 4



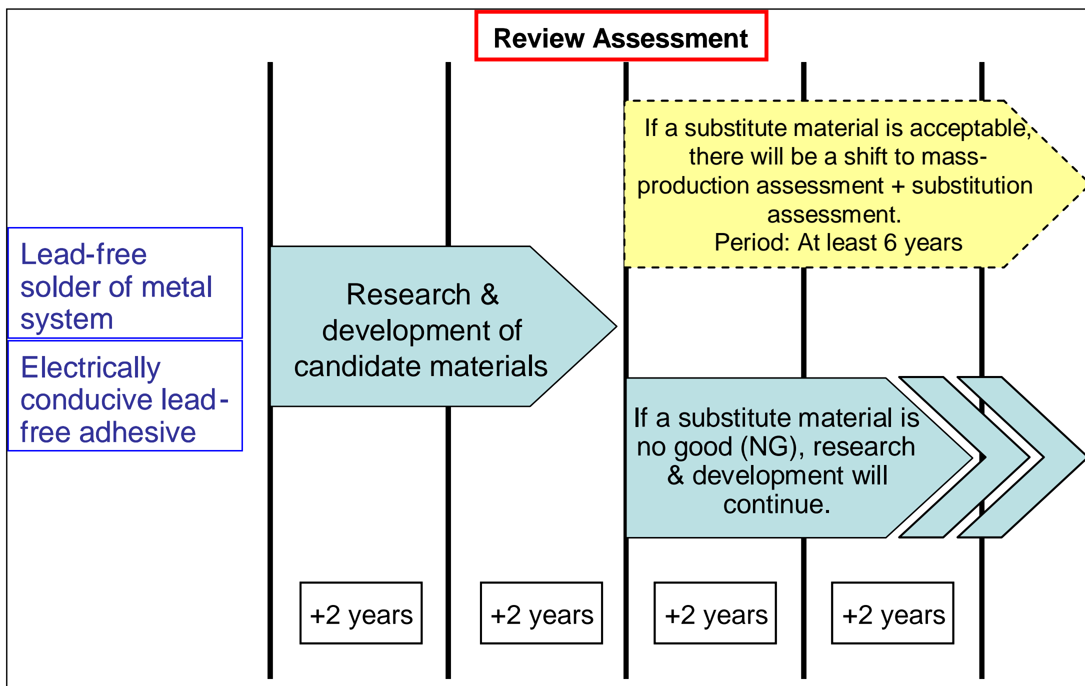
4. Please provide a roadmap specifying the necessary steps/achievements in research and development, including a time scale for the substitution or elimination of lead in this exemption.

<Answer 4>
ACEA et al. were asked to provide a roadmap for the substitution or elimination of Lead. ACEA et al.[iv] explains that for selected high power, high reliability and/or high-performance products, the ELV Exemption 8(g) will be required during the development and evaluation of substitute materials and interconnection technologies. Specifically, ACEA et al.[v] considers that Exemption 8(g) is necessary for a time period related to the following concerns:

- Until replacement materials and processes are successfully identified for large die, high power and long-term high reliability products;
- Until long term reliability is assessed and qualified under the harsh use conditions in vehicles according to automotive specifications (e.g. AEC-Q100); and
- Until products become available for automotive applications from a reasonable number of suppliers and in sufficient quantity.

ACEA et al.[vi] claims that after an automotive suitable Lead-free material is identified, and material / process development is frozen, usually a minimum of 6 years will be required to qualify the new material through the whole supply chain. Based upon the current status of these special products, it is not possible to estimate a transition date. Product delivery for replacement and repair will need to continue for the life of type approved vehicles**.**

Figure 9: Automotive Review Assessment Timeline



5. What is the amount of lead that will be contained in the applications in the scope of this exemption in vehicles
   a. placed on the EU market and
   b. worldwide

   in case the exemption remains valid beyond 2019? Please provide a substantiated estimate, clarifying how you have arrived at the stated result.

<Answer 5>

Flip chip applications are used in a few critical socketed products within the automotive industry. For competitive reasons the specific components / functions are not shared publicly. Examples of uses are provided in response to Question #1. From information that is available (OICA statistics), for 2017[vii] the Lead contained in an average vehicle ranges from 2mg to 35mg with 17mg /car as mean value. With15.7 million vehicles new registered in 2017 in the European Economic Area (EU28 +EFTA) the total Lead placed on the EU market making use of Exemption 8(g) is estimated with about 31kg to 548kg per year (2017)

Figure 10: Exemption 8(g) Lead in Vehicles Approximation

EU Vehicle Sales in 2017 [viii] ACEA Report						
Vehicle Type	**2017 Totals (Mio units)**		**Minimum amount of Pb per vehicle (mg)**	**Maximum amount of Pb per vehicle (mg)**	**Minimum total Pb (kg)**	**Maximum total Pb (kg)**
All	15,659		2	35	31	548

Additional remark for version made by ACEA :
With an average value of 17 mg/car and 15,7 Mio. vehicles put on EC market in 2017 we estimate a total Lead quantity of around 0,25 t/a for entry 8g applications.

6. Overall, please let us know whether you agree with the necessity to continue the exemption and sum up your arguments for or against its continuation.

   <Answer 6>
   The Exemption 8(g) of Annex II of Directive 2000/53/EC (ELV Directive) should be continued and substitution is not possible at this time.

   As seen from the responses to this set of questions, there are currently no Lead-free replacements available for flip chip applications requiring Exemption 8(g) within the automotive industry. The electronics industry will continue to investigate alternative Lead-free solutions/applications which meet the automotive requirements of form/fit/function based on AEC Q100 and AEC Q101 for products requiring the use of Exemption 8(g).

Appendix A

Table provided by JAPIA for 2 flip chip use cases

Use example of exemption 8(g) in JAPIA (2018.06.13)

Application	Component	Number of component per application	Mass of lead in component [mg]	Lead content in material [wt%]
Navigation	IC	1	2.48	37
Digital TV tuner	IC	1	5.34	36

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[i] http://elv.exemptions.oeko.info/index.php?id=64

[ii] References:
http://semimd.com/blog/2012/03/21/top-five-design-and-manufacturing-challenges-at-20nm/
"Citing International Business Strategies Inc. (IBS), a research firm, Cadence's Beckley said at the 32/28nm nodes, a fab runs $3 billion, process R&D is $1.2 billion, IC design costs ranges from $50 million to $90 million, and mask costs are from $2 million to $3 million"

[iii] References:
Tin/Lead and Lead-free solders comparison: Jean-Paul Clech, "Acceleration Factors and Thermal Cycling Test Efficiency for Lead-Free Sn-Ag-Cu Assemblies", SMTA International Conference, 2005.

[iv] Op. cit. ACEA et al. (2013b)

[v] Op. cit. ACEA et al. (2013b)

[vi] Op. cit. ACEA et al. (2013b)

[vii] Op. cit. OICA EU Statistics & sales figures EU28 (&EFTA) for 2017, (http://www.oica.net/category/sales-statistics/)